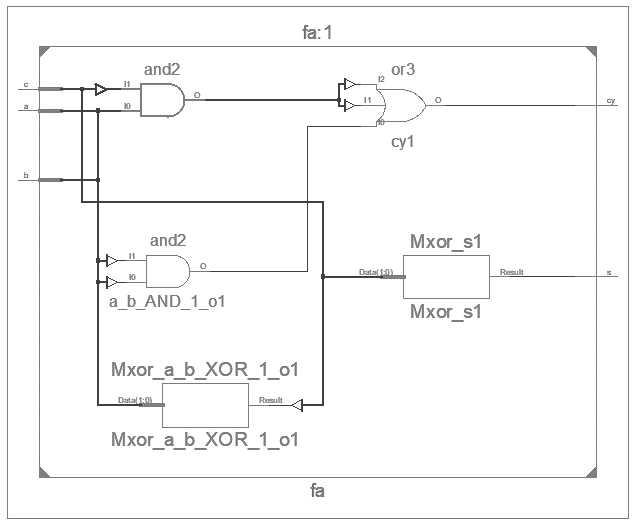
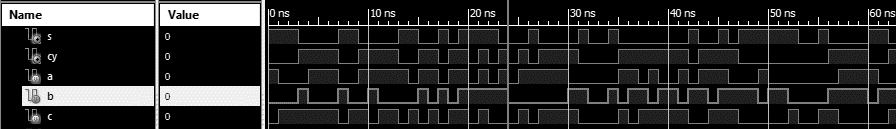
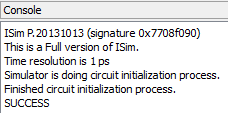
**RTL Diagram:**

****

**Output Waveform:**

****

**Simulation Output:**

****

**Experiment-2**

**Objective:**

To design a Single bit Full Adder and write a simple test bench for it. The test bench should generate stimulus to completely verify the functionality of the design.

**Tool Used:** Xilinx ISE.

**Theory:**

A full adder is a digital circuit that performs addition. Full adders are implemented with logic gates in hardware. A full adder adds three one-bit binary numbers, two operands and a carry bit. The adder outputs two numbers, a sum and a carry bit.

**Design Code:**

module fa(input a,b,c, output s,cy);

    assign s = a^b^c;

    assign cy = a&b | b&c | a&c;

endmodule

**Testbench Code:**

module tb();

    reg a,b,c;

    wire s,cy;

    integer x=0;

    fa dut(a,b,c,s,cy);

    initial begin

        repeat(100) begin

            {a,b,c} = $random;

            #1;

            if ({cy,s} != a+b+c) x = x+1;

        end

        if(!x) $display("SUCCESS");

        else $display("FAILURE");

    end

endmodule

**Result:**

The simulation output and the RTL diagram is observed and found to be valid.